Yimin Wang

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Education

National University of Singapore (NUS), Singapore — 2022—Present
Ph.D. student, Electrical and Computer Engineering — GPA: 4.83/5.0

Fudan University (FDU), Shanghai, China — 2019—2021
Ph.D. student, Microelectronics and Solid-state Electronics — GPA: 3.72/4.0

Jilin University (JLU), Changchun, China — 2015—2019
B.Sc., Electronic Information Science and Technology — GPA: 3.92/4.0

Research Interest

Circuits and systems; processing-in-memory architecture; hardware-software co-design for AI accelerator

Publications

In Preparation

- **[J4]** Y. Wang, YJ. Chong, Z. Wu, and X. Fong, "LLM Inference Acceleration on Scalable PIM Architecture with Balanced Dataflow and Fine-Grained Parallelism". (Extension from *ICCAD25*)
- **[J3]** Y. Wang and X. Fong, "Ising Machine with Asynchronous Latches and Boolean Logics for Versatile COP Solving". (Extension from *ISCAS24*)

Under Review

- **[J2]** Y. Wang, Z. Wu, YJ. Chong, and X. Fong, "JADE: Joint Architecture-Dataflow Exploration for LLM Inference on Heterogeneous In- and Near-memory Computing Systems", *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)*.

Accepted

- **[BC1]** Y. Wang and X. Fong, "Machine Learning Acceleration in Embedded Non-volatile Memory Subsystems for Edge Computing," *Non-Volatile Memory and Selector Devices: Technology and Applications*, Wiley, 2026.
- **[C4]** Y. Wang, YJ. Chong, and X. Fong, "LEAP: LLM Inference on Scalable PIM-NoC Architecture with Balanced Dataflow and Fine-Grained Parallelism," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2025.

Published

- **[C3]** Y. Wang and X. Fong, "Energy-Efficient Ising Machines Using Capacitance-Coupled Latches for MaxCut Solving," *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2024.
- **[C2]** Y. Wang, Y. Cen, and X. Fong, "Design Framework for Ising Machines with Bistable Latch-Based Spins and All-to-All Resistive Coupling," *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2024.
- **[J1]** Y. Wang and X. Fong, "Benchmarking DNN Mapping Methods for the In-Memory Computing Accelerators," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)*, 2023.
- **[C1]** Y. Wang, Z. Zou, and L. Zheng, "Design Framework for SRAM-Based Computing-In-Memory Edge CNN Accelerators," *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2021.

Work Experience

Research intern, **Advanced Micro Devices (AMD)**, Singapore — May 2024—November 2024

Awards

Third prize, 1st IEEE SEACAS Chipathon organized by IEEE CAS Society — Academic Year 2023-2024
Micron Foundation Prize, National University of Singapore — Academic Year 2021-2022
First-Class Scholarship, Fudan University — Academic Year 2019-2020
Outstanding Graduate, Jilin University — Academic Year 2018-2019
Samsung Scholarship, Jilin University — Academic Year 2017-2018
First-Class Scholarship, Jilin University — Academic Year 2015-2016, 2016-2017, 2017-2018

Teaching

Teaching assistant, CEG5202 Embedded Software Systems and Security, NUS — Spring 2023 and Spring 2024
Teaching assistant, CEG5201 Hardware Technologies, Principles, & Platforms, NUS — Fall 2023
Teaching assistant, TIE2030 Programming Methodology with Python, NUS — Fall 2022 and Fall 2023
Teaching assistant, TEE2101 Programming Methodology, NUS — Spring 2023
Teaching assistant, Internet of Things, FDU — Fall 2020

Academic Service

Committee member, IEEE Circuits and Systems Society (CASS), NUS Student Chapter — November 2023-Present
Reviewer, IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I) — January 2024–Present
Reviewer, IEEE Transactions on Very Large Scale Integration (VLSI) Systems — January 2024–Present
Reviewer, 2025 IEEE International Symposium on Circuits and Systems (ISCAS) — January 2025
Reviewer, 2024 ACM/IEEE International Conference on Computer-Aided Design (ICCAD) — June 2024